

Amendments to the Claims

1. *(Currently Amended)* A frequency divider comprising,
a first latch (10)-comprising a clock input for receiving a clock signal,
and
a second latch (20)-comprising a latch circuit configured as a low-pass filter, the second latch (20)-being crossed-coupled to the first latch.

2. *(Currently Amended)* A frequency divider as claimed in claim 1, wherein the second latch comprises
a differential pair of transistors (M1, M3; M2, M4)-including
a first pair of transistors comprising a first transistor (M1) coupled to second transistor (M3),
- second pair of transistor comprising third transistor (M2)-coupled to a fourth transistor (M4),
- each transistor having a drain, a source and a gate,
a drain of the first transistor (M1)-and a drain of the third transistor (M2)-being coupled to a source of the second transistor (M3)-and to a source of the fourth transistor (M4),-respectively
gates of the second transistor (M3)-and fourth transistor (M4)-receiving a signal generated by the first latch (10),
gates of the first transistor (M1)-and the third transistor (M2)-being coupled to a control signal (C1, C2),-for determining a low-pass characteristic of the second latch.

3. *(Currently Amended)* A frequency divider as claimed in claim 1, wherein the second latch comprises
a differential pair of transistors (M1', M2')-including
a fifth transistor (M1')-and a sixth transistor (M2'),
each transistor having a drain, a source and a gate,
- a drain of the fifth transistor (M1')-and the drain of the sixth transistor (M2')
being coupled to supply voltage (Vs) via respective resistors,

a source of the fifth transistor (~~M1'~~) and a source of the sixth transistor (~~M2'~~) being coupled to a common potential, gates of the fifth transistor (~~M1'~~) and sixth transistor (~~M2'~~) receiving a signal generated by the first latch (~~I0~~).

4. (*Currently Amended*) A frequency divider as claimed in claim 2, wherein the control signal (~~C1, C2~~) is a DC signal.

5. (*Currently Amended*) A frequency divider as claimed in claim 2, wherein the control signal (~~C1, C2~~) is a complementary clock signal to the clock signal supplied to the first latch (~~I0~~).

6. (*Currently Amended*) A frequency divider as claimed in claim 5, wherein the first latch (~~I0~~) is substantially identical to the second latch (~~I2~~).

7. (*Currently Amended*) A frequency divider as claimed in ~~any of the preceding claims 2-6~~ claim 2, wherein each latch comprises a negative resistance coupled between the drains of said second transistor (~~M3~~) and said fourth transistor (~~M4~~), and between the drain of the fifth transistor (~~M1'~~) and drain of the sixth transistor (~~M6'~~), respectively.